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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/655,363	09/04/2003	John G. Edelen	2001-0886.01	1567

21972 7590 02/14/2006

LEXMARK INTERNATIONAL, INC.
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EXAMINER	
NGUYEN, LAMSON D	

ART UNIT	PAPER NUMBER
2861	

DATE MAILED: 02/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/655,363	EDELEN ET AL.	
	Examiner	Art Unit	
	Lamson D. Nguyen	2861	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *RCE dated 12/01/05*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 10, 14, 16, 25, and 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carrigan (6,546,177) in view of Conta (6,371,589) and Ishinaga et al. (US 2002/0149657).

Carrigan teaches an inkjet head (figure 1b) and a method of controlling the temperature of the printhead (figure 28), resistor elements to the heat the printhead (column 35, lines 20-31; figure 31, element 3115), a controller of the resistor element (figure 1b, element 124), and temperature sensors operatively connected to the controller to enable the controller to monitor the chip temperature the resistors to heat the chip.

Carrigan fails to teach a silicon substrate, MOS logic blocks, and the sense resistors implanted in the silicon substrate.

Meanwhile, Conta et al disclose a printhead chip consisting of MOS logic blocks (column 1, lines 53-60), a silicon substrate (figure 2, silicon substrate 10) and Ishinaga teaches a diode embedded in a silicon substrate (figure 22, substrate 620, diodes 622 and 623).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Carrigan to incorporate the teaching of silicon substrate, MOS logic blocks, and embedded diode taught by Conta and Ishinaga, respectively,

for the purpose of integrating several components of a printhead using fewer manufacturing steps and thereby reducing power consumed, supporting a printhead and detecting printhead's temperature, respectively.

Claims 2-9, 11-13, 15, 17-24, and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carrigan in view of Conta and Ishinaga as applied to claims 1 and 16 above, and further in view of Tanaka et al (US 2002/0060333), Aswell (US 2001/0050410), and Stanley Wolf, Silicon Processing for the VLSI era, volume 2, lattice press, 1990, pages 354-356.

Carrigan in view of Conta and Ishinaga disclose all claimed features of the invention except a TCR of at least .004 ohms/degree C.

Aswell discloses that the TRC may range from 600-6000 ohms/degrees C (.0006 to .006 ohms/degrees C), paragraph 0038 and that the thickness of the resistor is 1um, paragraph 0007. The length and width of the resistors depend on the sheet resistance and would be obtained with the formula of paragraph 0005; if one dimension is chosen, the other is thereby obtained, making the resistor footprint a matter of design choice.

Stanley Wolf discloses lightly doped drains (LDD) in making CMOS devices using PSD and NSD material, table 5.2, page 355. Given Carrigan and Conta teachings of CMOS technology, LDD would have been used for its known function of their channel effects.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use material having the sheet resistance of Tanaka, the TCR of Aswell and the materials of Wolf to make the implanted TSR of Carriagn, Conta, and Ishinaga in order to obain a TSR having a resistance variation of a magnitude to be detectable above the noise

level of the printhead chip yet being small enough to be associated with each nozzle of the printhead.

Response to Arguments

Applicant's arguments filed 12/01/05 have been fully considered but they are not persuasive.

On page 3, paragraph 2 of the arguments, the applicants argued that Ishinaga does not teach the diodes are implanted into the substrate and that the applicants suggested that the diodes of Ishinaga could be formed by techniques other than implantation. The examiner would like to point out that claims 1-15 are apparatus claims and therefore, only structural limitations would be given patentable weight. In this regard, how the diodes get into the substrate is irrelevant. The fact is the diodes are disposed inside the substrate as clearly seen in figure 22 of Ishinaga. Claims 16-31 are directed to a method of controlling the temperature of an inkjet chip where one of the steps includes "implanting temperature sense resistors in the substrate of the chip". The applicants argued that Ishinaga is silent as to how the diodes are disposed in the chip. According to Webster's II New Riverside University Dictionary, the definition of "implant" is "to set in firmly or embed". Again, figure 22 of Ishinaga clearly shows that diodes 622 and 623 are set in or embedded within the substrate 620.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lamson D. Nguyen whose telephone number is 571-272-2259. The examiner can normally be reached on 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Talbott can be reached on 571-272-1934. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LAMSON NGUYEN
PRIMARY EXAMINER
02/09/06